

ABSTRACT

In recent system LSIs, a plurality of RAMs differing in capacity and in bit width have come to be mounted on a single chip according to the needs on the system side. However, when testing the plurality of RAMs, if the RAMs differ in capacity, they cannot be tested using the same test pattern (for example, HALF-MARCH) even if a special pin is provided for each RAM, because X, Y address mapping differs between the different RAMs; accordingly, the test has to be performed by dividing the RAMs into groups each consisting of RAMs having the same memory space, and this has lead to increased test time. An external address signal and a test-only address signal are provided as RAM control signals and, in the latter case, the number of X, Y addresses in each of the RAMs 4 and 5 is set equal to that of the largest capacity RAM 3 within the same chip, thereby making the X, Y address mapping the same for all the RAMs 3 to 5.